REMARKS

This is a full and timely response to the outstanding Action mailed December 14, 2005. Upon entry of the amendments in this response, claims 1-3 5, 7-11, 13, 15-17, 19, 21-25, 27 and 29-34 remain pending. In particular, Applicant has amended claims 1, 9, 15, 23 and 29 without waiver, disclaimer or prejudice to the previously claimed subject matter. In the amended claims 1, 9, 15, 23 and 29, the limitation "adjacent to the gate" has been added. As this subject matter was clearly supported by the original application, no new matter has been added to the application by this amendment. For at least the reasons set forth below, reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections under 35 U.S.C. 103

The Office Action rejected claims 1-3, 5, 7, 15-17, 19, and 21 under 35 U.S.C 103(a) as allegedly unpatentable over Akaishi et al. (US Pat. 6,207,518) in view of Williams et al. (US Pat. 5,055,896); that claims 8, 22 and 34 stand rejected under 35 U.S.C 103(a) as allegedly unpatentable over Akaishi in view of Williams, and further in view of Williams et al. (US Pat. 5,514,608); that claims 9-11, 13, 23-25, and 27 stand rejected under 35 U.S.C 103(a) as allegedly unpatentable over Akaishi in view of Williams, Ito et al. (US Pat. 5,856,695) and Williams'608. Applicant respectfully requests reconsideration and withdrawal of the rejections for at least the reasons that follow.

With respect to Akaishi, Akaishi discloses an N-channel transistor structure comprising a p-type body region 3, an n-type diffused region 4 within the p-type body region 3, an n-type diffused region 5 apart from the n-type diffused region 4, a gate electrode 7 on the surface of a substrate 1, a drift region 22 composed of a shallow region 22A below the gate electrode 7, and a

deep region 22B in the vicinity of the and n-type diffused region 5, a LOCOS oxide film 9 between the gate electrode 7 and the deep region 22B of the drift region 22, and a p-type disused region 12 within the p-type body region 3 (See col. 1, lines 21-50 and Fig. 10A).

In pertinent part, the Office Action alleged that the difference between Akaishi and the claimed invention is having no field oxide between the gate and first and second wells, but that the reference can be combined with Williams, which teaches a field plate 34 instead of a field oxide region between the gate and the second well, for the purpose of reducing stress-created defects in the crystalline structure at the drift region/channel interface 28 (See col. 2, lines 47-51). Applicant respectfully disagrees. In fact, Williams discloses there are no stress-created defects in the crystalline structure at the drift region/channel interface 28 by eliminating the formation of **a LOCOS field oxide near the drift region/channel interface 28** (see col. 2, lines 47-51 and Fig. 2). In the disclosure of Akaishi, however, the LOCOS oxide film 9 is located apart from the junction of the p-type body region 3 and the drift region 22 (i.e. the drift region/channel interface) by the length of the shallow region 22A of the drift region 22 (See Fig. 10A). Accordingly, there is no reason to eliminate the LOCOS oxide film 9 because the drift region/channel interface is not in proximity therewith.

Moreover, with respect to Williams, Williams discloses an N-channel LDD lateral DMOS transistor comprising an N-drift region 10 self-aligned with a gate 18, using the gate 18 as a mask, and field oxide 32 is formed over the entire surface of the wafer (See col. 2, lines 42-47 and fig. 2). That is, there is no junction between the P body region 20 and the drift region 10. However, in the disclosure of Akaishi, there is a junction between the p-type body region 3 and the drift region 22 (fig. 10A). Accordingly, Applicants respectfully submit that, even combined, Akaishi and Williams fail to disclose all of the claimed features. Further, there is no proper

motivation to combine the teachings of Akaishi and Williams due to different doped region arrangement therebetween. For at least these reasons, the rejections should be withdrawn.

Additionally, Williams teaches a field oxide 32 is formed over the entire surface of the wafer (See col. 2, lines 46-47 and Fig. 2). That is, a field oxide 32 is formed adjacent to the gate 18 and between the gate 18 and the N-drift region 10. After combing Akaishi and Williams, it is still required to form a field oxide adjacent to the gate and between the gate and the drift region. Note that what the teaching of Williams is to change the arrangement of the field oxide, rather than actually eliminate the field oxide from the semiconductor device or lateral DMOS device.

Turning now to the amended claims, claim 1 recites:

1. A high voltage device comprising:
a substrate;
first and second wells respectively of a first type and a second type in the substrate;
a gate formed on a junction between the first and second wells, without a field oxide adjacent to the gate and between the gate and the first and second wells;
first and second doped regions both of the second type, respectively formed in the first and second wells and on both sides of the gate;
a third doped region of the first type in the first well and adjacent to the first doped region; and
a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate, wherein the fourth lightly doped region is shallower than the first doped region.

(*Emphasis Added*).

Similarly, claim 9 recites:

9. A high voltage device formed on a P substrate comprising:
an HVNMOS comprising:
first P and N wells in the P substrate;
a first gate formed on a junction between the first P and N wells, without a field oxide adjacent to the first gate and between the gate and the first P and N wells;
two first N+ doped regions respectively formed in the first P and N wells, and on both sides of the first gate;

a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and
an N lightly doped region adjacent to the first N+ doped region in the first P well and beneath the first gate ; and
a HVPMOS comprising:
an N+ buried layer in the P substrate;
second N and P wells in the P substrate and above the N+ buried layer;
a second gate formed on a junction between the second N and P wells, without a field oxide adjacent to the second gate and between the gate and the second P and N wells;
two second P+ doped regions respectively formed in the second N and P wells, and on both sides of the second gate;
a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well; and
a P lightly doped region adjacent to the second P+ doped region in the second N well and beneath the second gate.

(*Emphasis Added*).

Likewise, claim 15 recites:

15. A method for manufacturing a high voltage device, comprising the steps of:
providing a substrate;
forming first and second wells respectively of a first type and a second type in the substrate;
forming a gate on a junction between the first and second wells, without a field oxide formed adjacent to the gate and between the gate and the first and second wells;
forming first and second doped regions both of the second type, respectively in the first and second wells and on both sides of the gate;
forming a third doped region of the first type in the first well and adjacent to the first doped region; and
forming a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate, wherein the fourth lightly doped region is shallower than the first doped region.

(*Emphasis Added*).

Claim 23 recites:

23. A method for manufacturing a high voltage device comprising the steps of:
providing a substrate;
forming a HVNMOS on the P substrate by:
forming first P and N wells in the P substrate;

forming a first gate on a junction between the first P and N wells, without a field oxide formed adjacent to the first gate and between the first gate and the first P and N wells;
forming two first N+ doped regions respectively in the first P and N wells, and on both sides of the first gate;
forming a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and
forming a N lightly doped region adjacent to the first N+ doped region in the first P well and beneath the first gate; and
forming a HVPMOS on the P substrate by:
forming an N+ buried layer in the P substrate;
forming second N and P wells in the P substrate and above the N+ buried layer;
forming a second gate on a junction between the second N and P wells, without a field oxide formed adjacent to the second gate and between the second gate and the second P and N wells;
forming two second P+ doped regions respectively in the second N and P wells, and on both sides of the second gate;
forming a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well; and
forming a P lightly doped region adjacent to the second P+ doped region in the second N well and beneath the second gate.

(*Emphasis Added*).

Finally, independent claim 29 recites:

29. A high voltage device comprising:
a substrate;
first and second wells respectively of a first type and a second type in the substrate;
a gate formed on a junction between the first and second wells, without a field oxide adjacent to the gate and between the gate and the first and second wells;
first and second doped regions both of the second type, respectively formed in the first and second wells and on both sides of the gate;
a third doped region of the first type in the first well and adjacent to the first doped region; and
a fourth lightly doped region of the second type next to the first doped region and beneath the gate.

(*Emphasis Added*).

According to MPEP 2143, to establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Moreover, the prior reference (or references when combined) must teach or suggest all the claim limitations. As set forth above, Applicant respectfully asserts that Akaishi and Williams does not teach or reasonably suggest at least the features/limitations that have been emphasized above in independent claims 1, 9, 15, 23 and 29. More specifically, in combining these references, the Office Action stated only that the combination would have been obvious "for the purpose of reducing stress created defects in the crystalline structure at the drift region/channel interface." (Office Action, page 3). This alleged motivation is clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicants note that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order

to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a high-voltage MOS device, as claimed by the Applicant.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference

with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000).

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, those rejections should be withdrawn.

As there is no motivation to combine Akaishi and Williams, Applicant respectfully asserts that the rejections of independent claims 1, 9, 15, 23 and 29 are deficient and that these claims are in condition for allowance. Further, as dependent claims 2-3, 5, 7 and 8 incorporate the limitations of claim 1, dependent claims 10-11 and 13 incorporate the limitations of claim 9, dependent claims 16-17, 19, and 21-22 incorporate the limitations of claim 15, dependent claims 24, 25, and 27 incorporate the limitations of claim 23, and dependent claims 30-34 incorporate the limitations of claim 29, Applicants respectfully submit that these claims also are in condition for allowance.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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